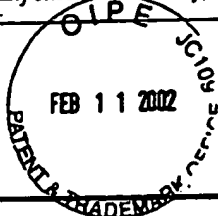


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Page 1 of 5	First Named Inventor: Benjamin S. Ting	
	Filing Date: December 5, 2001	



U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		4,020,469		Marrung Technology Center	2104-26-77	
		4,661,901		Veneski	4-28-87	
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		4,720,780		Dolecek	1-19-88	
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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
		EP	0415542 A1	A1	Advanced Micro Devices, Inc.	03/06/91		
		EP	0630115 A2	A2	Pilkington Micro-Electronics Limited	12/21/94		
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		GB	2295738 A		Altera Corporation	06/05/96		

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		5,550,782		Cliff et al.	8-27-96	
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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
		WO						
		PCT	WO94/10754	A1	Xilinx, Inc.	05/11/94		
		PCT	WO95/04404	A1	Advantage Logic, Inc.	02/09/95		

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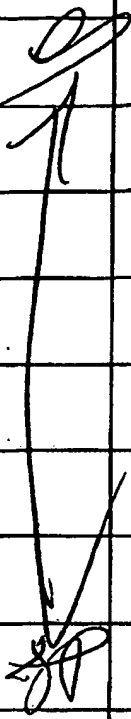
Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 1207P006D	Application Number: 10/021,744
Page 4 of 5		First Named Inventor: Benjamin S. Ting	
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OTHER ART - NO PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
e		RICHARD CLIFF et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.3.1-7.3.5.	
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		BUFFOLI et al., "Dynamically Reconfigurable Devices used to Implement a Self-Tuning, High Performance PID Controller", IEEE 1989, pp. 107-112.	
		DEVADAS, S., "Boolean Decomposition of Programmable Logic Arrays", IEEE 1988, pp. 2.5.1-2.5.5.	
		VIDAL, J., "Implementing Neural Nets with Programmable Logic", IEEE 1988, pp. 50-53.	

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Examiner Initials*	Cite No ¹		Translation ²
		YACHYANG SUN et al., "An Area Minimizer for Floorplans with L-Shaped Regions", 1992, Int'l. Conference on Computer Design, pp. 383-386.	
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		Xilinx, "The Programmable Gate Array Data Book", 1992	
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